IN THE CLAIMS

1-5 (Cancelled)

6. (Currently amended) The method of claim [[5]]8, wherein the thickness of the amorphous silicon capping layer is not less than 50 Å.

7. (Currently amended) The method of claim [[5]]8, wherein the silicide layer comprises tungsten silicide.

8. (Previously presented) A method for forming a control gate electrode layer of a semiconductor device electrode in which a gate insulation layer, a polysilicon layer for a floating gate electrode, and an intergate dielectric layer are sequentially stacked on a semiconductor substrate, the method comprising:

a) forming an amorphous silicon layer on the intergate dielectric layer;

b) annealing the amorphous silicon to form a polysilicon layer;

c) forming an amorphous silicon capping layer on the polysilicon layer; and

d) forming a silicide layer on the capping layer, using dichlorosilane, wherein the silicide layer comprises tungsten silicide, and wherein forming the tungsten silicide layer comprises;

supplying a first silane (SiH_4) gas to a process chamber in which a wafer including the thin film of amorphous silicon is loaded;

supplying a dichlorosilane (SiH_2Cl_2) gas and a tungsten hexafluoride (WF_6) gas to the process chamber to deposit the tungsten silicide layer on the capping layer;

purging the dichlorosilane (SiH_2Cl_2) gas and the tungsten hexafluoride (WF_6) gas from the process chamber; and

supplying a second silane (SiH_4) gas to the process chamber.

9. (Currently amended) The method of claim [[5]]8, wherein the annealing is performed in a nitrogen ambient.

10-16 are (Cancelled)